This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1(Original). An under bump metallization structure applicable to be disposed on bonding pads of a semiconductor wafer, wherein a passivation layer covers the wafer and exposes the bonding pads, the under bump metallization structure comprising:

an adhesive layer formed on the bonding pads;

a first barrier layer disposed on the adhesive layer;

a wetting layer formed on the first barrier layer; and

a second barrier layer disposed on the wetting layer, wherein a material of the second barrier comprises tin and nickel.

2(Original). The structure of claim 1, wherein the quantity of the tin is smaller than the quantity of the nickel.

3(Previously Presented). The structure of claim 1, wherein the first barrier layer comprises nickel-vanadium or nickel.

4(Original). The structure of claim 1, wherein the wetting layer is a copper layer.

Claim 5(Canceled).

6(Previously Presented). The structure of claim 1, wherein the adhesive layer comprises titanium.

7(Original). The structure of claim 1, wherein the thickness of the second barrier layer is ranged from about 50 μm to about 80 μm.

8(Currently Amended). A semiconductor wafer applicable to a flip chip device, comprising:

an active surface;

a plurality of bonding pads formed on the active surface;

a passivation covering the active surface and exposing the bonding pads;

a first electrically conductive layer formed on the bonding pads, wherein the first electrically conductive layer comprises a titanium layer, a nickel-vanadium layer alloy layer and a copper layer and the titanium layer is directly attached to the bonding pads; and

a second electrically conductive layer formed on the first electrically conductive layer, wherein the second electrically conductive layer comprises tin and nickel.

9(Original). The semiconductor wafer of claim 8, further comprising a plurality of bumps formed above the bonding pads and attached to the second electrically conductive layer.

10(Original). The semiconductor wafer of claim 8, wherein the second electrically conductive layer is extended above the active surface.

11(Original). The semiconductor wafer of claim 8, further comprising a dielectric layer covering the second electrically conductive layer and exposing a portion of the second electrically conductive layer to form a redistributed pad.

12(Original). The semiconductor wafer of claim 11, further comprising a bump formed on the redistributed pad.

Claims 13 and 14(Canceled).

15(Previously Presented). The semiconductor wafer of claim 11, wherein a material of the dielectric layer comprises polyimide.

16(Original). The semiconductor wafer of claim 8, wherein the quantity of the tin is smaller than the quantity of the nickel.

17(Previously Presented). The semiconductor wafer of claim 8, wherein the thickness of the second electrically conductive layer is ranged from about 50 μm to about 80 μm.

18(Previously Presented). The semiconductor wafer of claim 11, wherein a material of the dielectric layer comprises Benzocyclobutence.

Claim 19(Canceled).

20(New). A semiconductor wafer applicable to a flip chip device, comprising:

an active surface;

a plurality of bonding pads formed on the active surface;

a passivation covering the active surface and exposing the bonding pads;

a first electrically conductive layer formed on the bonding pads, wherein the first electrically conductive layer comprises an aluminum layer, a nickel-vanadium layer alloy

layer and a copper layer and the aluminum layer is directly attached to the bonding pads; and

a second electrically conductive layer formed on the first electrically conductive layer, wherein the second electrically conductive layer comprises tin and nickel.

9(Original). The semiconductor wafer of claim 8, further comprising a plurality of bumps formed above the bonding pads and attached to the second electrically conductive layer.

21(New). The semiconductor wafer of claim 20, further comprising a plurality of bumps formed above the bonding pads and attached to the second electrically conductive layer.

22(New). The semiconductor wafer of claim 20, wherein the second electrically conductive layer is extended above the active surface.

23(New). The semiconductor wafer of claim 20, further comprising a dielectric layer covering the second electrically conductive layer and exposing a portion of the second electrically conductive layer to form a redistributed pad.

24(New). The semiconductor wafer of claim 20, wherein the quantity of the tin is smaller than the quantity of the nickel.